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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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EXAMINER	
ECKERT II,G	
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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary

Application No.	Applicant(s)
09/421,322	Oi et al.
Examiner	**Art Unit**
George C. Eckert II	2815

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Oct 18, 1999* .

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above, claim(s) *2, 4, and 7* is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *1, 3, 5, 6, and 8* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☒ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on *Oct 18, 1999* is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13) ☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☒ All b) ☐ Some* c) ☐ None of:

1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)

16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). *2 & 3*

18) ☐ Interview Summary (PTO-413) Paper No(s). _____

19) ☐ Notice of Informal Patent Application (PTO-152)

20) ☐ Other:

DETAILED ACTION

Election/Restriction

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1, 3, 5, 6 and 8, drawn to a semiconductor device, classified in class 257, subclass 347.

   II. Claims 2, 4, and 7, drawn to a method of making a semiconductor, classified in class 438, subclass 149+.

2. The inventions are distinct, each from the other because of the following reasons: Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make another and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the dielectrically separated silicon islands can be formed by a CMP or etch-back method.

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

4. During a telephone conversation with G. Lloyd Knight a provisional election was made prosecute the invention of Group I, claims 1, 3, 5, 6 and 8. Affirmation of this election must be made by applicant in replying to this Office action. Claims 2, 4 and 7 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

5. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a petition under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(I).

Priority

6. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

7. Figures 13, 14, 15A-J, 16 and 17 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

Specification

8. The disclosure is objected to because of the following informalities: the *Background of the Invention* section, pages 1-7, makes reference to "conventional" drawings but the figures referenced are applicant's purported invention (e.g. page 5, line 6, page 6, lines 26 and 29). Also, the remainder of the specification should be reviewed for similar occurrences (e.g. page 25, line 28, fig. 6 or fig. 7?). Appropriate correction is required.

9. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

10. Claims 6 and 8 are objected to because of the following informalities: With regard to claim 6, on line 2 delete the first occurrence of "the" and insert --a-- in its place because flatness was not earlier defined. Also, on line 2, delete "these" and insert --the--. With regard to claim 8, on line 1, delete "fabrication method for a" and on line 2, delete the first occurrence of "the" and insert --a-- in its place because flatness was not earlier defined. Also, on line 2, delete "these" and insert --the--. Appropriate correction is required.

Claim Rejections - 35 U.S.C. § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

11. Claims 3, 6 and 8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. With regard to claim 3, the preamble does not make clear the structure of applicant's invention in light of that taught by in the specification. That is, the limitation of "a plurality of polysilicon island mutually separated by a dielectrically separating oxide film" does not

make clear if the polysilicon islands are those islands on which active devices are later formed or if the polysilicon islands are merely those islands between the single crystal islands, as taught in the specification, in which devices are formed. For this Office action, the latter interpretation will be used. With regard to claims 6 and 8, the claim does not make clear what "value" is being referred to such that a "maximum" or a "minimum" can be determined.

Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim Rejections - 35 U.S.C. § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 1 and 5 are rejected under 35 U.S.C. 102(b) as being anticipated by US 5,420,064 to Okonogi et al. Okonogi et al. teach, with reference to figures 2 and 3A-E, a dielectrically

separated wafer having a plurality of dielectrically separated silicon islands 11a, mutually defined by a dielectrically separating oxide film 13 on the surface of the wafer, wherein the dielectrically separated islands 11a comprise:

a high concentration impurity layer 12 (col. 3, lines 27-29) formed on the bottom of the islands; and

a low concentration impurity layer (the remainder of 11a) having an identical conductivity (n-, col. 3, lines 21-24) laminated on the high concentration layer.

With regard to claim 5, Okonogi et al., with reference to figures 2 and 3A-E, a dielectrically separated wafer having a plurality of dielectrically separated silicon islands 11a, insulated by a dielectrically separating oxide film 13 on the wafer surface, the dielectrically separated wafer comprises a surface between one dielectrically separated silicon island and another neighboring dielectrically separated silicon island formed so as to be flat (see figure 3E for example which shows the area between islands 11a as flat).

13. Claims 3, 6 and 8 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Okonogi et al. With regard to claim 3 as best understood, Okonogi et al. teach a dielectrically separated wafer having a polysilicon layer 14 and a plurality of polysilicon islands mutually separated by a dielectrically separating oxide film 13 formed on the surface of the polysilicon layer (those regions of polysilicon layer 14 which, in figure 3E for example, are shaped as triangles) wherein:

the polysilicon layer is formed on the dielectrically separating oxide film 13.

Regarding the limitation that the polysilicon layer has a seed layer grown by low temperature CVD, this limitation is considered a processing limitation which does not structurally differentiate over Okonogi et al. and is thus considered anticipated by Okonogi et al. In the alternative, the limitation is considered merely an obvious processing variant over that taught by Okonogi et al., is considered within the skill of a mechanic in the art and is an obvious choice depending on the working limitations available to the manufacturer (e.g., if low temperature processes are required to avoid migration of dopants in other areas within the wafer).

With regard to claims 6 and 8 as best understood, as discussed above, Okonogi et al. teach the limitations of claim 1 and teach or make obvious the limitations of claim 3. Okonogi et al. did not expressly disclose that a flatness on the surface of the dielectrically separated islands is less than 0.2 μm when measured by a stylus-profilometer. However, this limitation is also considered either taught by Okonogi et al. or, in the alternative, obvious over the same. That is, Okonogi et al. teach that the wafer is "abraded and polished" (col. 3, lines 45-49) to form the islands. As such, it is considered inherent that the polishing will create a surface having no difference between the maximum and minimum values of flatness. In the alternative, it is considered obvious that the surface of the device of Okonogi et al. would be formed to have a flatness as instantly claimed. Though Okonogi et al. do not expressly disclose any value of a surface roughness, it is considered within the skill of a mechanic in the art to minimize any surface roughness as motivated by the relationship, known in the art, between surface roughness and complications of processing

subsequent layers (alignment issues, planarity issues affecting wiring parameters, etc.). Therefore, claims 6 and 8 are considered either inherent or obvious over that taught by Okonogi et al.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. All cited references teach the general state of the art regarding applicant's invention.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to George C. Eckert II whose telephone number is (703) 305-2752.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mr. Eddie Lee can be reached on (703) 308-1690. The fax phone number for this Group is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.

GCE
September 17, 2001

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800